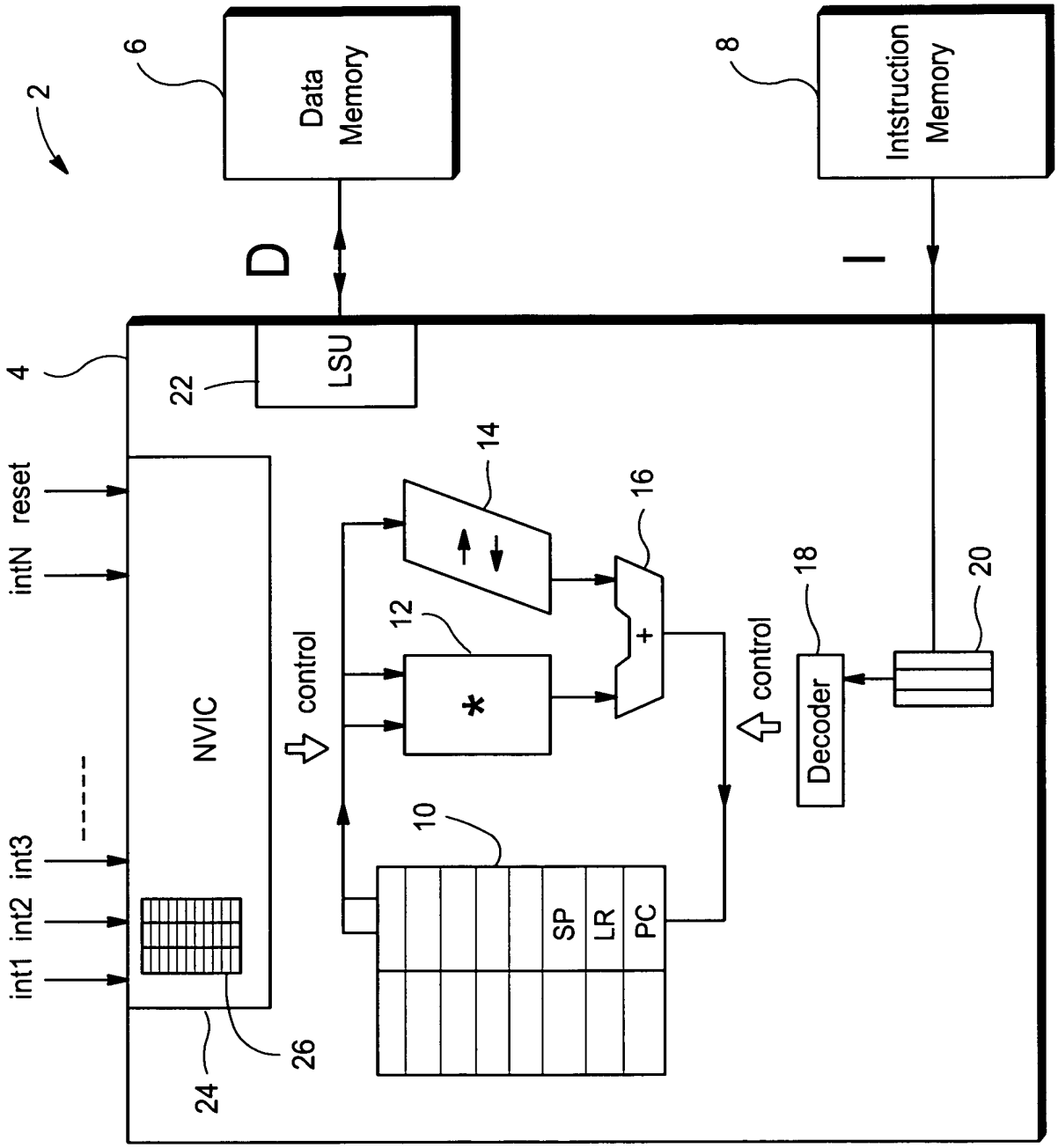

Fig. 1

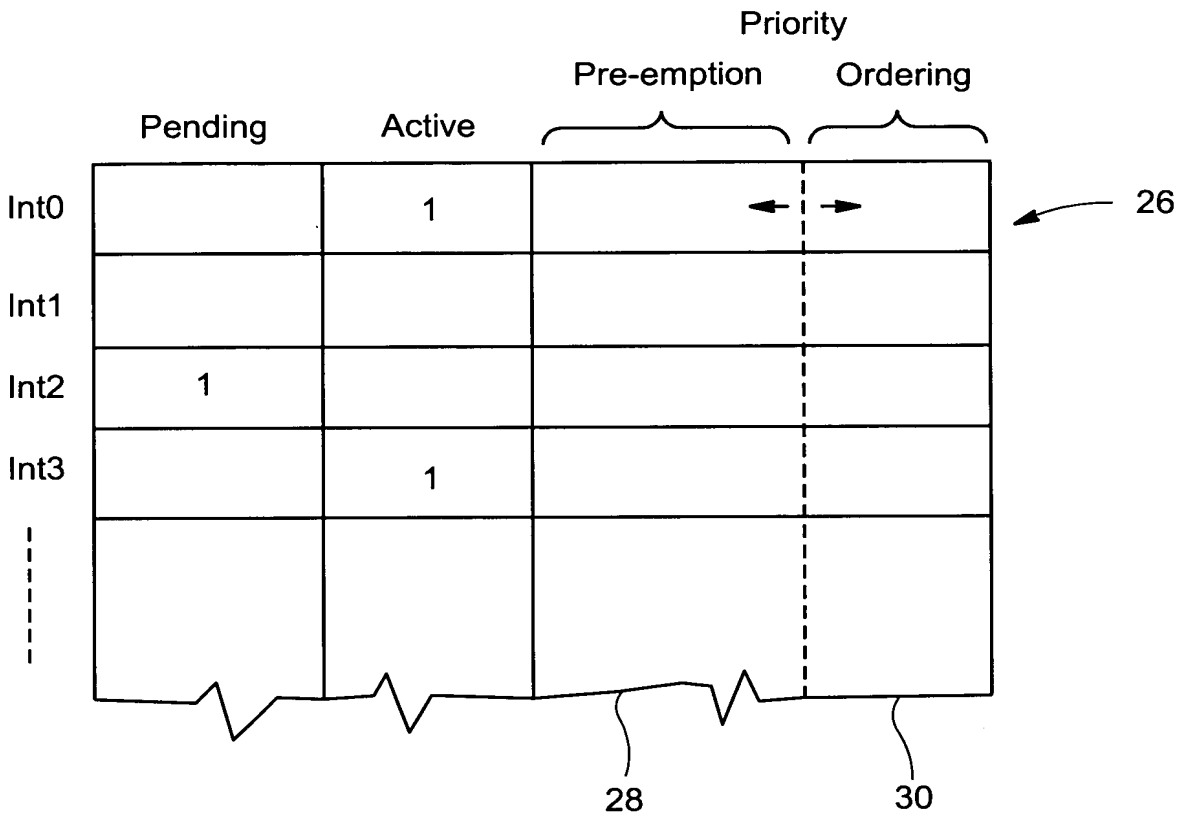
NVIC Control Table
Priority
Pre-emption
Ordering
Pending
Active
Int0
Int1
Int2
Int3
1
1
1
26
28
30

Fig. 2

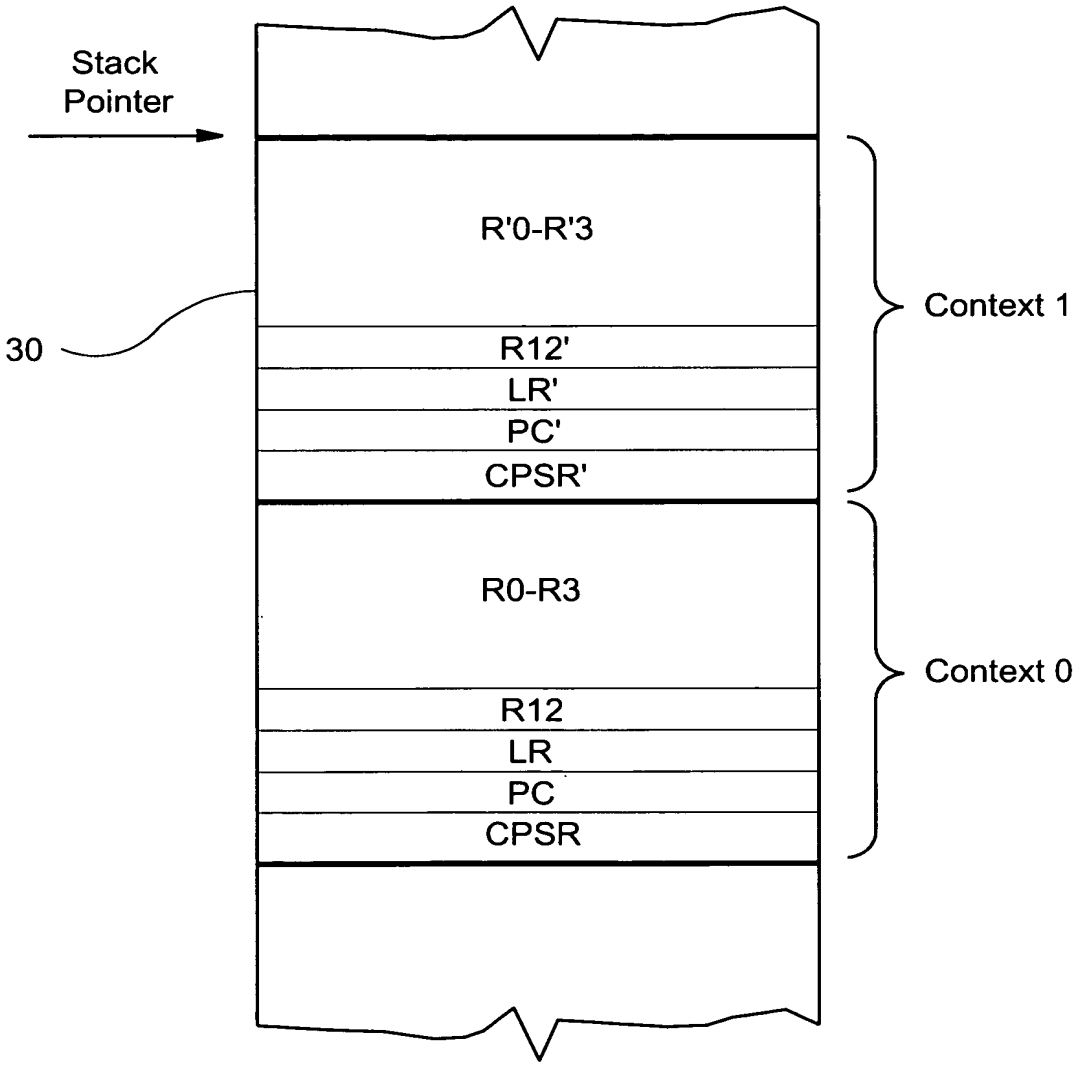
Stack Memory
Stack Pointer
30
R'0-R'3
R12'
LR'
PC'
CPSR'
Context 1
R0-R3
R12
LR
PC
CPSR
Context 0

Fig. 3

Priority Inversions

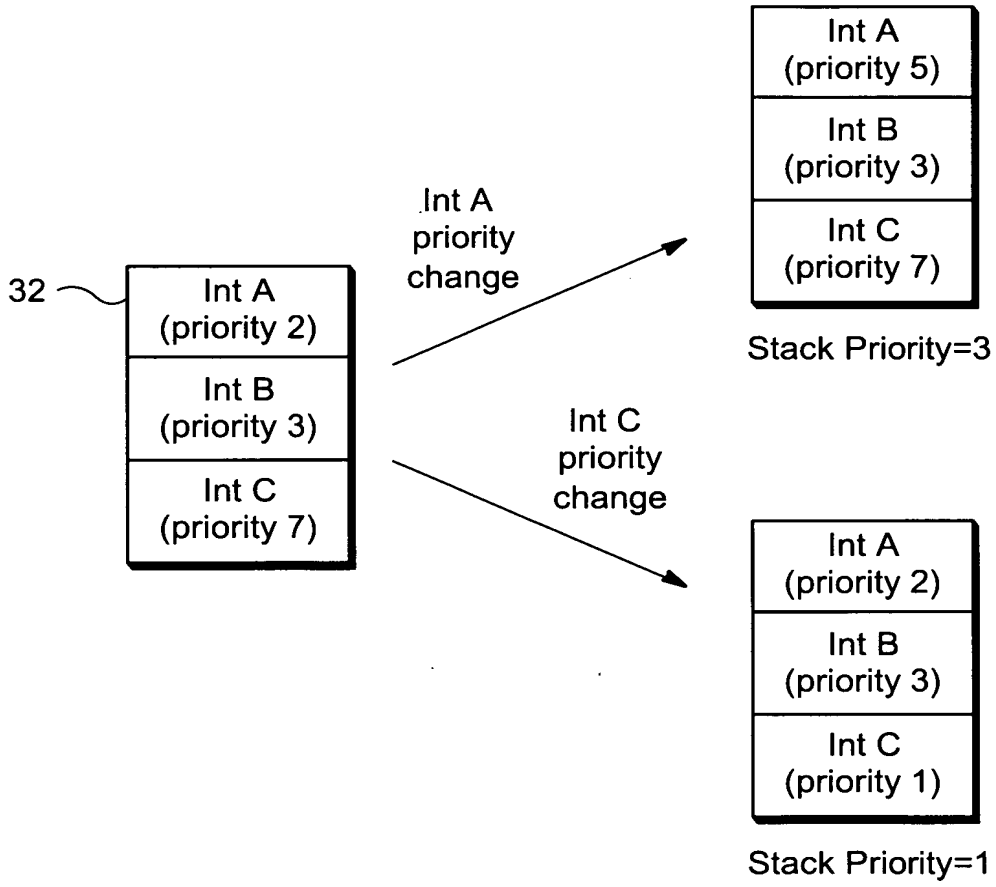

Fig. 4

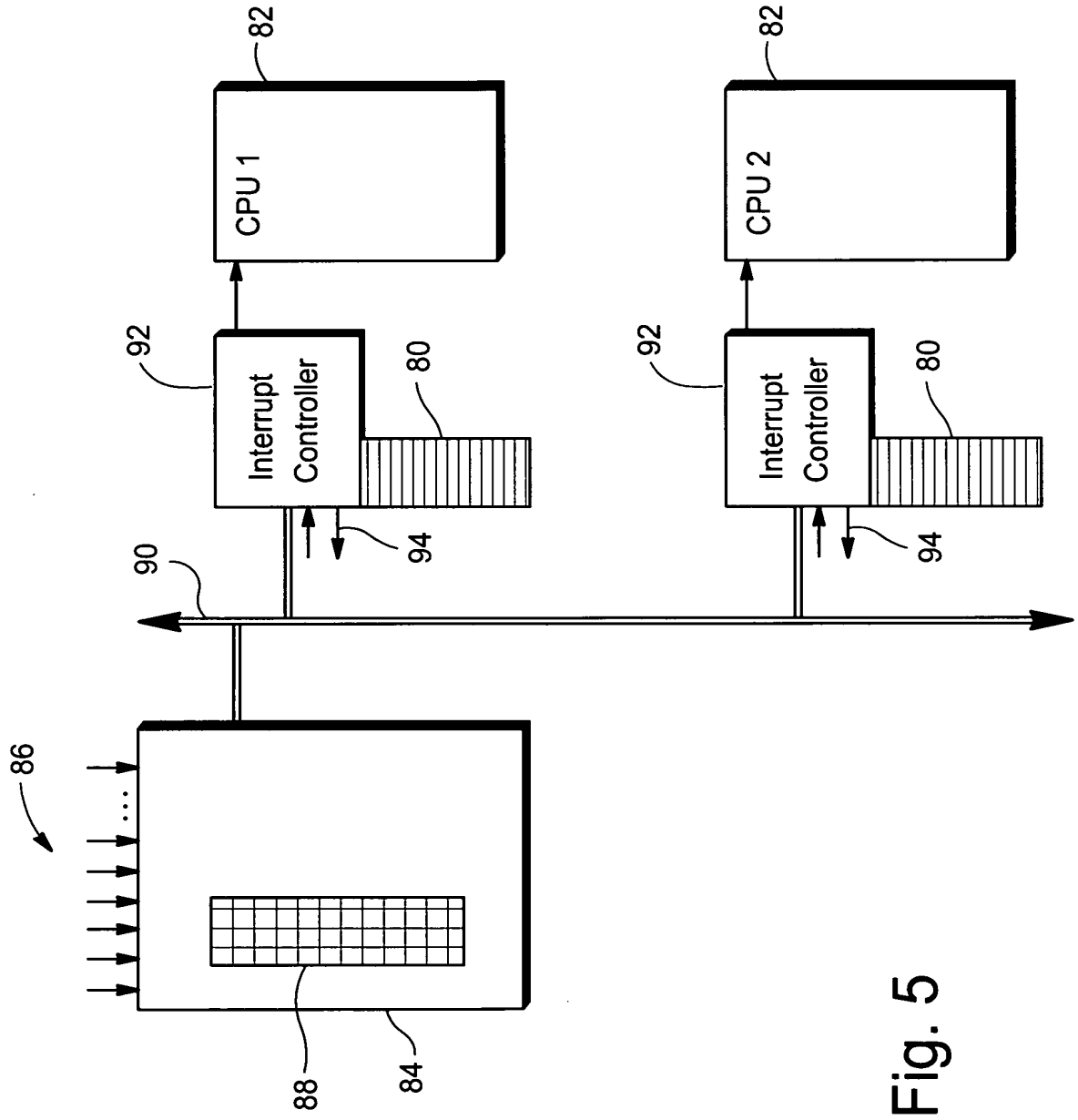
82
CPU 1
82
CPU 2
92
Interrupt Controller
80
92
Interrupt Controller
80
94
94
90
86
88
84

Fig. 5

Main Flow

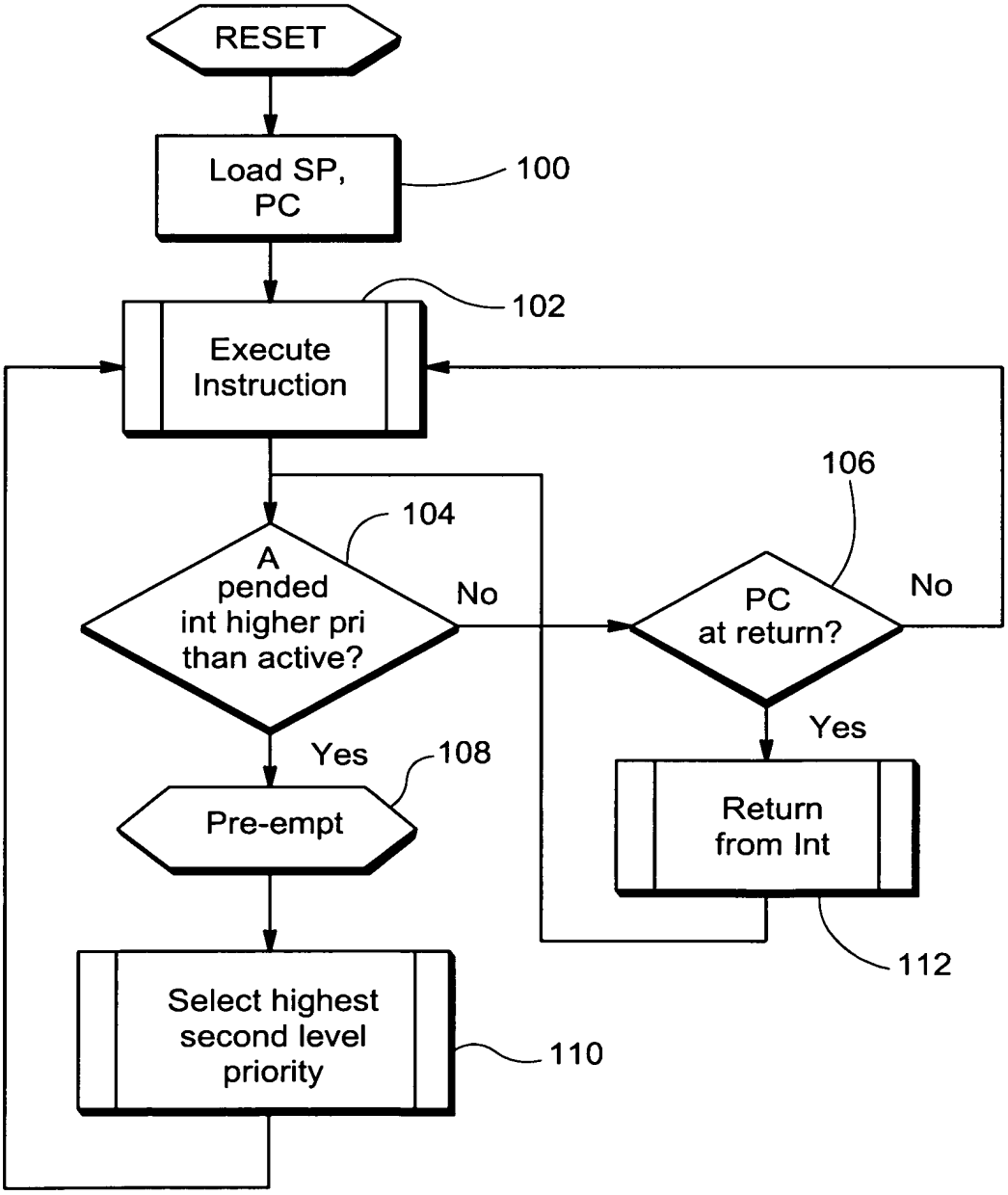

Fig. 6

Main Flow with Tail Chaining

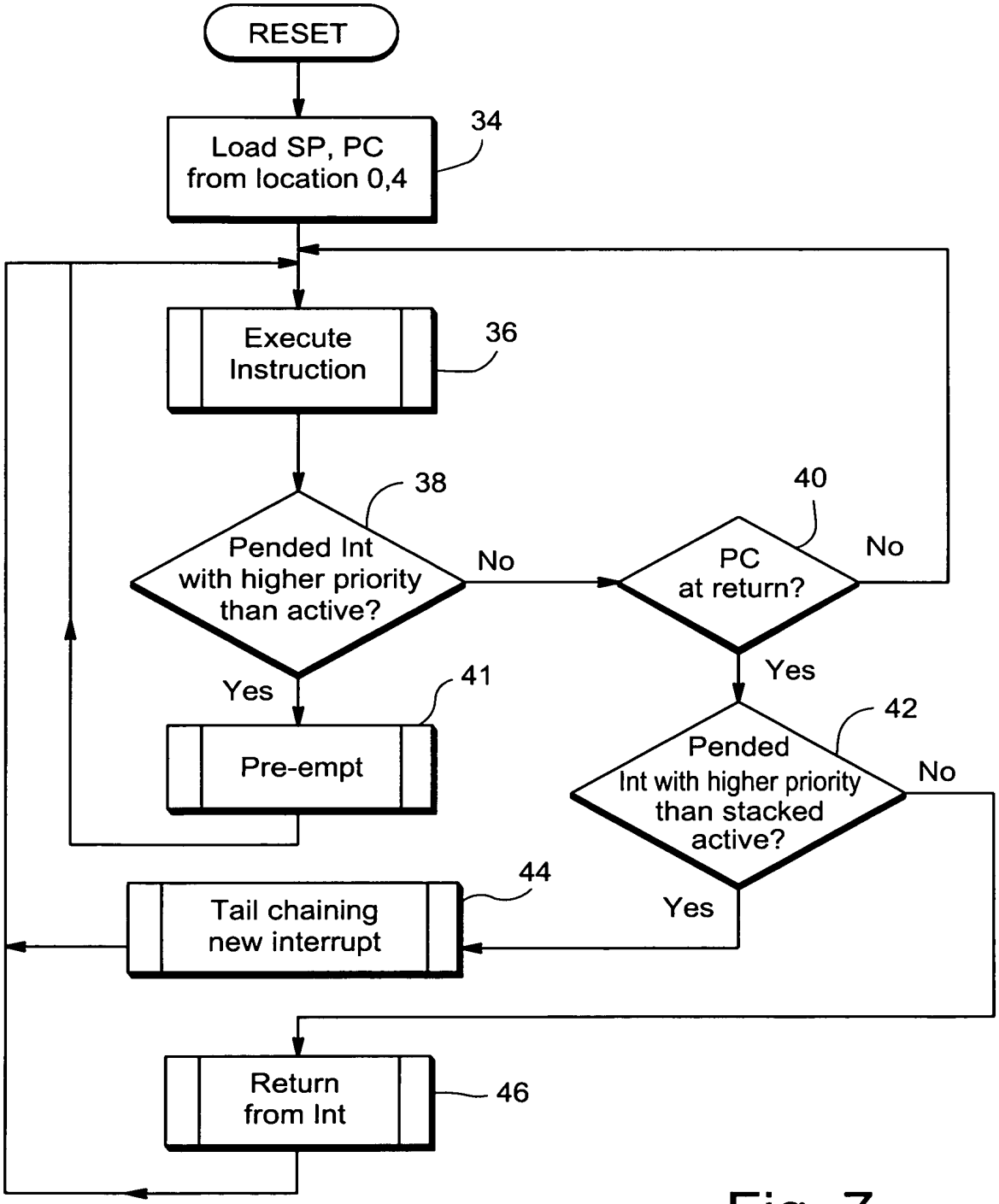

Fig. 7

Pre-emption Flow

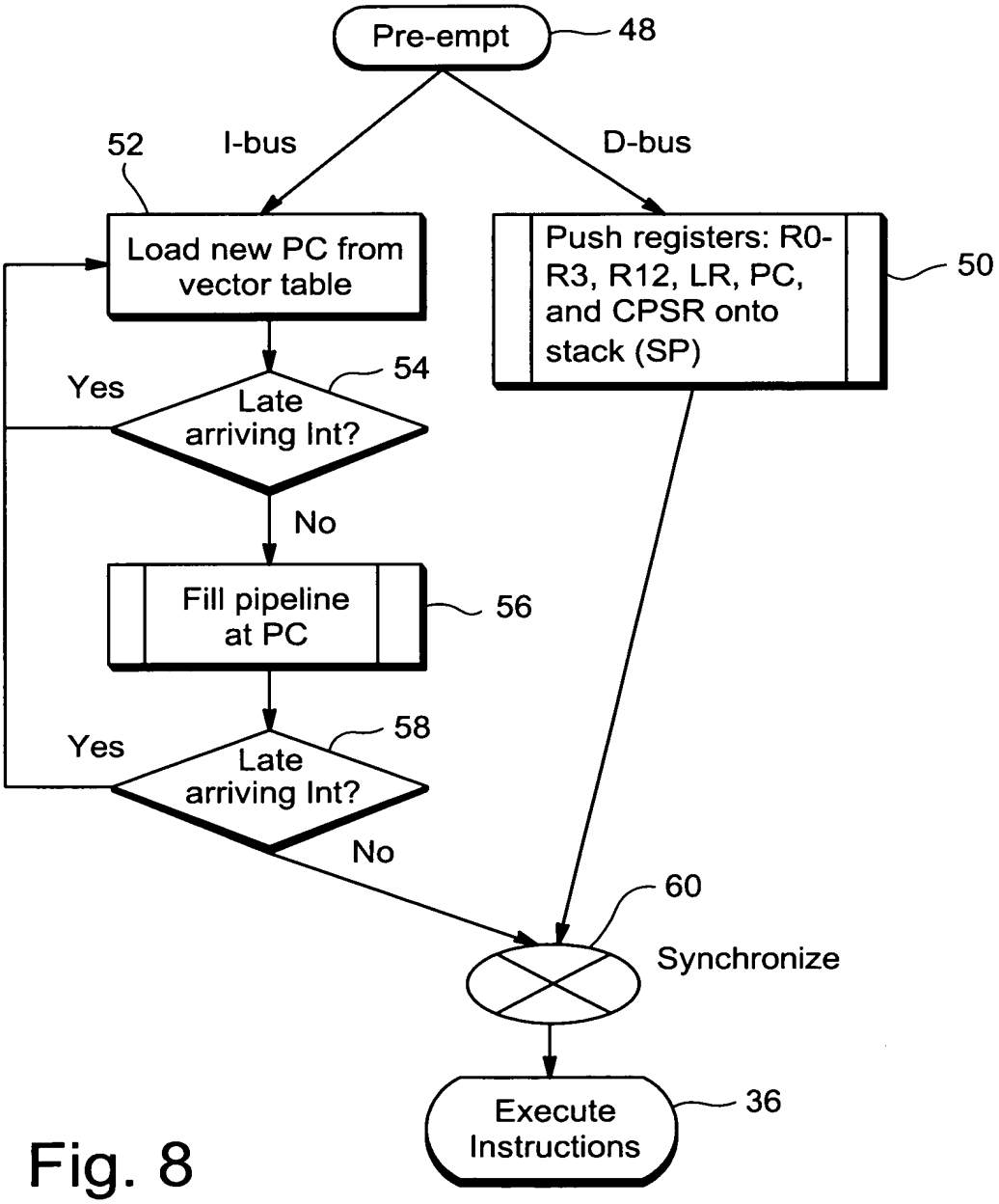

Fig. 8

Return From Interrupt Flow

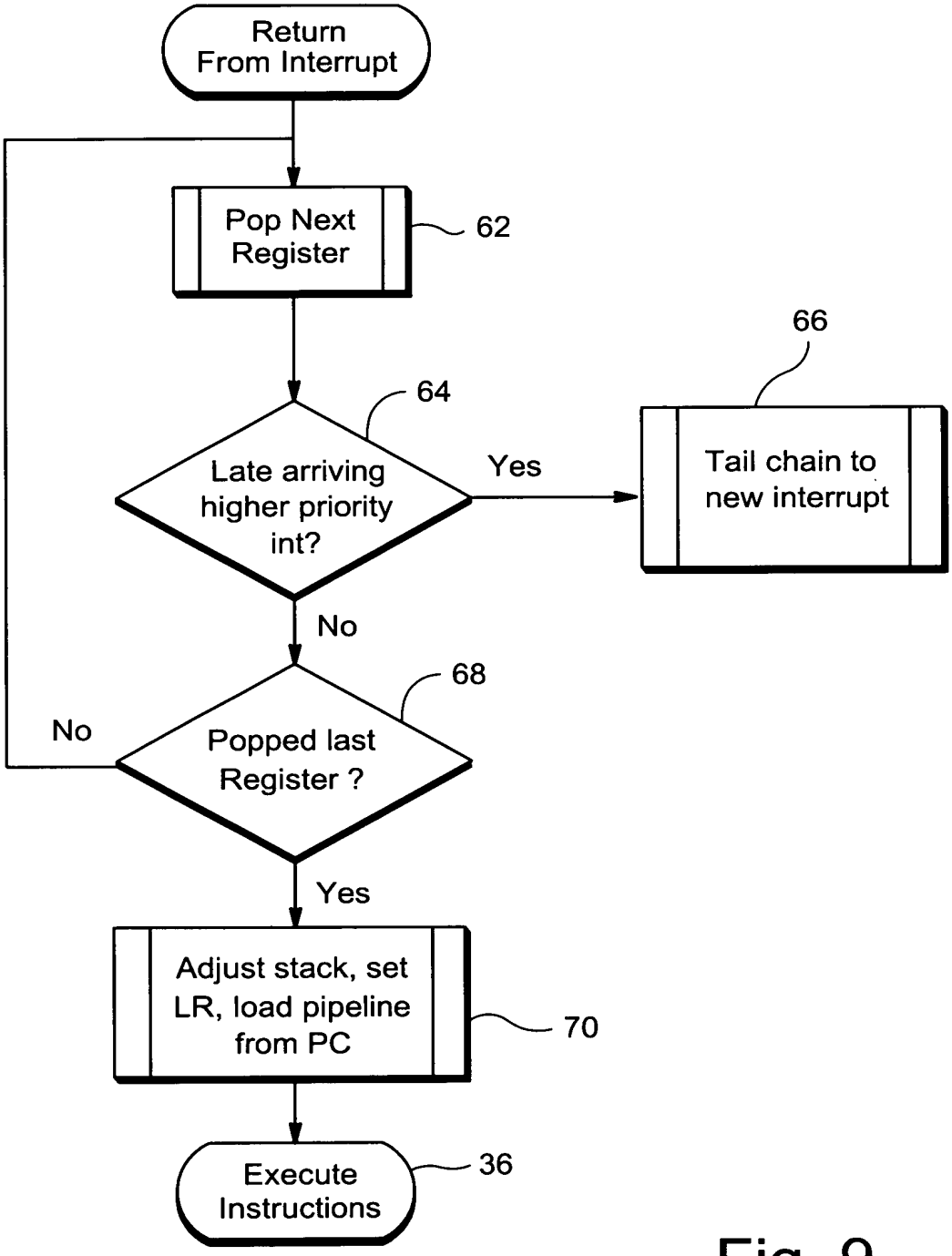

Fig. 9

Tail Chaining Flow

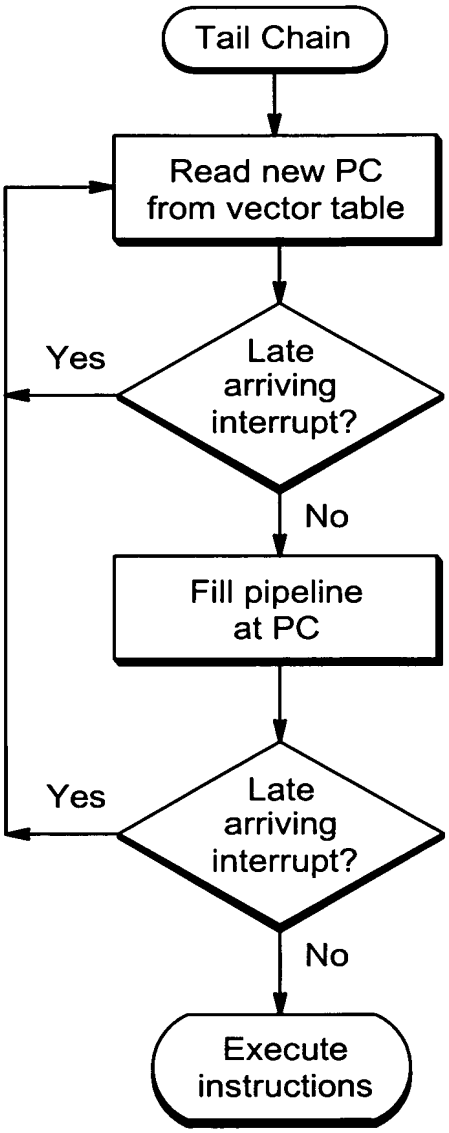

Fig. 10